M1503 Hardware Design

Version：V1.0

Version History

Date	Version	Description of change	Author
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CONTENTS

1 **About this document**

1.1 Applicable scope ..... 错误！未定义书签。

1.2**Writing purpose**

1.3 Support and reference documents list ..... 错误！未定义书签。

1.4 Abbreviation ..... 错误！未定义书签。

2 PRODUCT DESCRIPTION **5**

2.1 mechanics properties **5**

2.2 Product function description **8**

2.2.1 Baseband function 8

2.2.2 Radio frequency function ..... **错误！未定义书签。**

3 INTERFACE DESCRIPTION **11**

3.1 Pin definition **11**

3.1.1 Pin I/O parameter definition 11

3.1.2 Pin configuration diagram ..... **错误！未定义书签。**

3.1.3 Pin description ..... **错误！未定义书签。**

3.2 word Condition ..... 错误！未定义书签。**8**

3.3 Interface level characteristic ..... 错误！未定义书签。**7**

3.3.1 Digital level signal characteristic ..... **错误！未定义书签。**

3.4 Power supply interface ..... 错误！未定义书签。9

3.4.1 Power supply pin description **19**9

3.4.2 Power supply requirements ..... 错误！未定义书签。9

3.5 USIM card interface **20**

3.5.1 Pin description **20**

3.5.2 electrical specification **20**

3.5.3 USIM card interface application **21**

3.6 USB Interface **21**

3.6.1 Pin description **21**

3.6.2 Electrical character **21**

3.6.3 USB Interface application **22**

3.7 I2S Interface **22**

3.7.1 Pin description **22**

3.8 UARTInterface **22**

3.8.1 Pin description **22**

3.8.2 UARTInterface electrical properties **23**

3.9 Open / shut down and reset interface ..... 错误！未定义书签。

3.9.1 Pin description ..... 错误！未定义书签。

3.9.2 Interface application ..... 错误！未定义书签。5

3.10 Analog audio interface ..... 错误！未定义书签。**5**

3.10.1 Pin description.....错误！未定义书签。
3.10.2 Interface application.....错误！未定义书签。6
3.10.3 Audio signal PCB.....错误！未定义书签。7
3.11 Camera interface.....错误！未定义书签。**7**
3.11.1 Pin description.....错误！未定义书签。7
3.11.2 Interface application.....错误！未定义书签。8
3.12 LCD interface.....错误！未定义书签。**9**
3.12.1 Pin description.....错误！未定义书签。9
3.12.2 Interface application.....**30**
3.13 Antenna interface.....**32**
3.13.1 Antenna signal Go line rule.....**32**
3.13.2 Interface application.....**32**

4 PRODUCT ELECTRICAL CHARACTERISTICS 33

4.1 Power source.....**33**
4.1.1 Power supply.....**33**
4.1.2 Switch machine process.....**33**
4.1.3 Reset process.....**34**

5 DESIGN GUIDANCE 34

5.1 General design rules and requirements.....**34**
5.2 Power supply circuit design.....**35**
5.3 RF circuit design.....**35**
5.3.1 Initial attention to antenna design.....35
5.4 EMC and ESDdesign suggestion.....**36**
5.5 PCBPad design.....**37**
5.6 Thermal design suggestion.....错误！未定义书签。**8**
5.7 Product promotion plan.....错误！未定义书签。

6 PRODUCTION GUIDANCE ..... 错误！未定义书签。

6.1. Steel net design.....**39**
6.2. Temperature curve.....错误！未定义书签。

1 About this document

1.1 Applicable scope

This document describes LCCModule of 4G (hereinafter referred to as M1503), the basic specifications, product electrical characteristics, design guidance and hardware interface development guidance. Users need to follow this documentation requirements and guidance for design.

This document applies only to M1503 products in the application development.

1.2 Writing purpose

This document provides the design and development basis for the product users. By reading this document, users can have a whole understanding of the product, the technical parameters of the product have a clear understanding, and can be used in this document to complete the development of wireless 4G Internet access functions.

This hardware development document not only provides the product functional features and technical parameters, but also provides product reliability testing and related testing standards, business functions to achieve process, RF performance indicators and user circuit design guidance.。

1.3 Support and reference documents list

In addition to the hardware development documentation, we also provide a guide to the development board based on this product manual and software development instruction manual, 1-1 is supported as a list.

Table 1-1 support document list

Serial number	Document name
1	《M1503 module software user manual》
2	《M1503 Module development board user manual》

1.4 Abbreviation

Table 1-2 is the document related to abbreviations and, English explained.

Table **错误！文档中没有指定样式的文字。**-1List of acronyms

Abbreviation	English full name
ESD	Electro-Static discharge
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver Transmitter
SDC	Secure Digital Controller
USIM	UniversalSubscriber Identification Module
SPI	Serial Peripheral Interface
I2C	Inter-Integrated Circuit
PCM	Pulse-coded Modulation
I/O	Input/output
LED	Light Emitting Diode
GPIO	General-purpose Input/Output
GSM	Global Standard for Mobile Communications
GPRS	General Packet Radio Service
WCDMA	Wideband Code Division Multi© Access
UMTS	Universal Mobile Telecommunication System
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
AGPS	Assisted Global Positioning System
BER	Bit Error Rate
DL	Downlink
DPCH	Dedicated Physical Channel
DPCH_Ec	Average energy per PN chip for DPCH. DPCH

2 Product description

This product is a LCCModuleof 4G wireless internet module, with the speed, small size, light weight, high reliability can be widely used in various products and devices with wireless internet access:

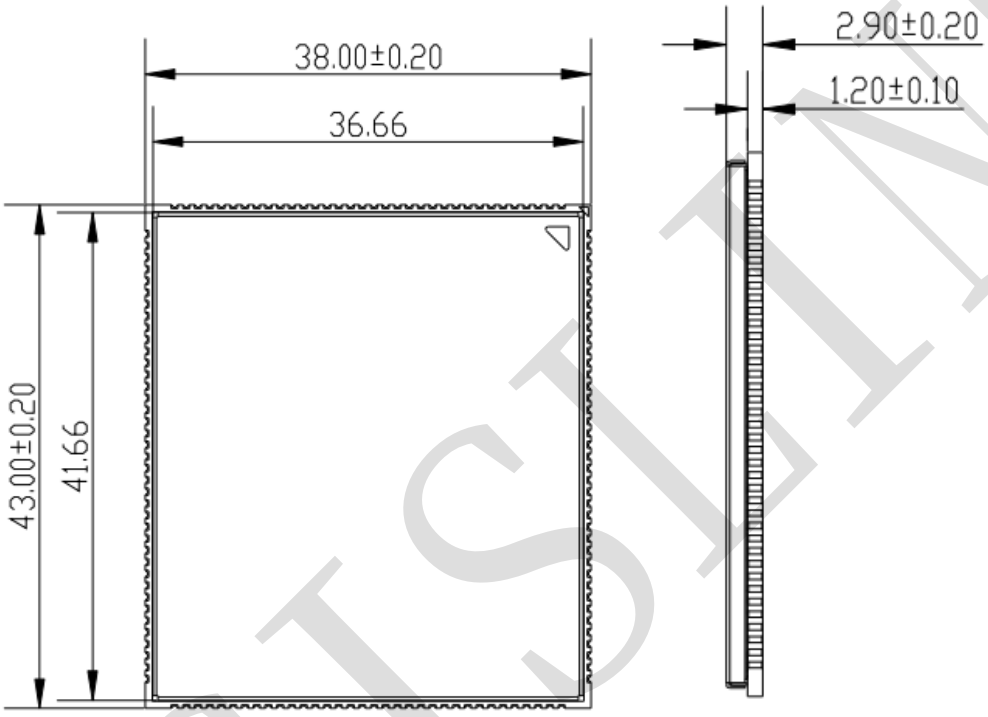
- Support:
  FDD-LTE: B1/B3/B7/B8/B20；
  TDD-LTE: B38/B39/B40/B41
  WCDMA/DC-HSPA+：B1/B2/B5/B8
  TD-SCDMA：B34/B39
  GSM/GPRS/EDGE：GSM850MHz/GSM900MHz/DCS1800MHz/PCS1900MHz
  CDMA/EVDO:BC0
  BT: BT4.0+BR/EDR+BLE
  FM: RX only, Support RDS
  WIFI: 802.11a/b/g/n 2.4/5G
  GPS: GPS/GLONASS/BEIDOU
  A-GPS: Support
  Provide USIM card interface（3.0V/1.8V）；USB2.0 Interface、UART Interface、PCM Interface、PCM Interface、GPIO Interface、Analog audio port etc.；
- Can provide mobile environment GSM/GPRS/EDGE, UMTS/HSDPA/HSUPA high-speed data access services;
- Dimensions（L×W×H）:43mm×38mm×3.0mm

TOP BOTTOM

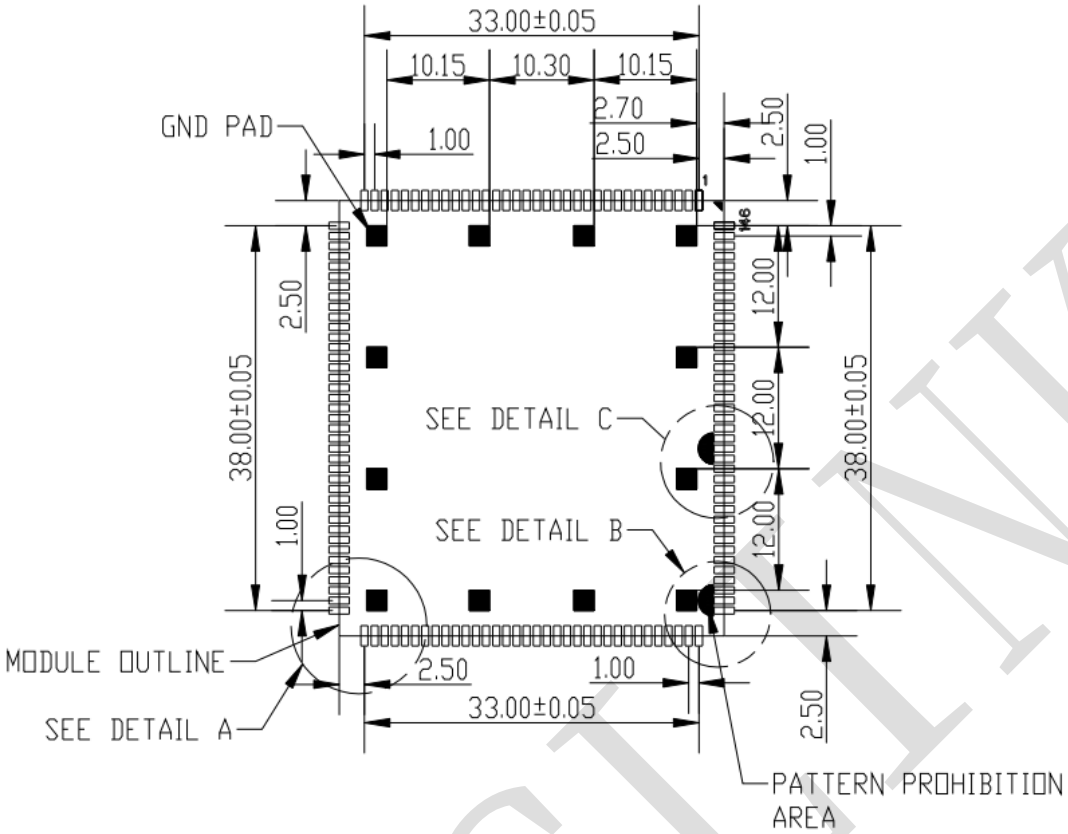
Figure错误！文档中没有指定样式的文字。-1Product physical map

2.1 Mechanics Characteristic

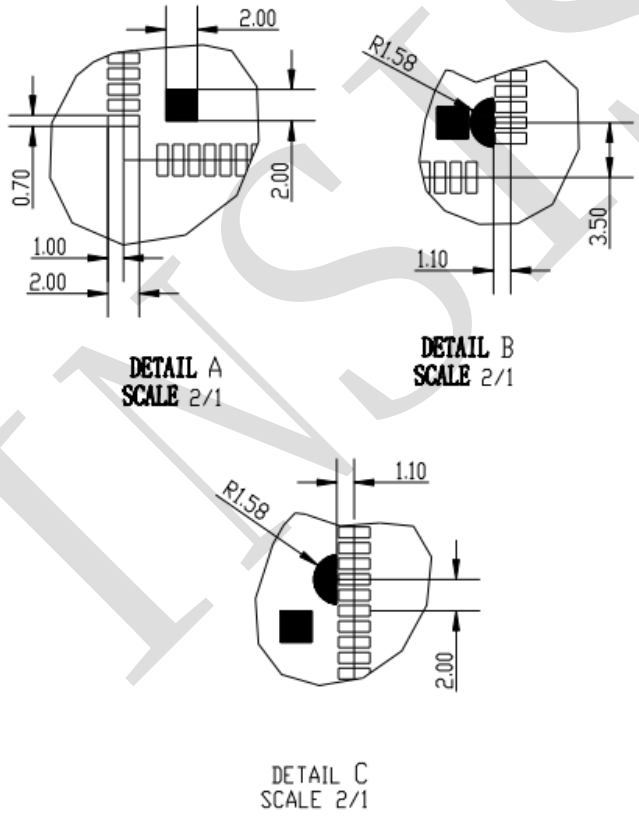
The product module is 146-PIN LCC package module, in addition to signal pin, also contains many special heat welding disc to improve joint performance, mechanical strength and heat dissipation performance, the heat release welding disc 25 and uniform distribution in the bottom of the PCB. Package size is 43 x 38 mm, the height is 3.0mm.Pin 1 position from the bottom of the belt angle welding plate to identify, the missing corner where the direction of the corresponding module angle pad, figure 2-2 is the product dimension type map:



(a)Top dimension (b) Thickness



(c) PIN LCC foot size（Bottom view）



(d) Detail

Figure错误！文档中没有指定样式的文字。-2Module size

2.2 Product function description

2.2.1 Baseband function

The baseband part of this product mainly includes the following signal group：USBInterface signal、USIM cardInterface signal、I2CInterface signal、UARTInterface signal、I2S Interface signal、UARTInterface signal、Analog audio interface、Module startup、Power supply and ground，Figure 2-3 is a system connection frame diagram.

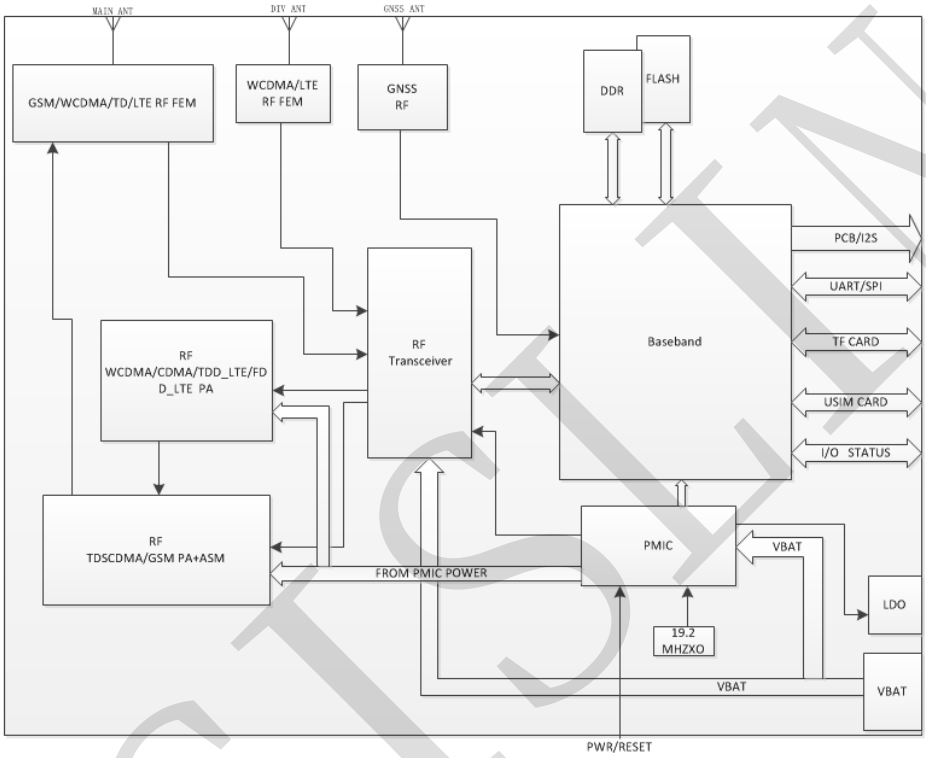


Figure 2-3 system connection frame structure diagram

2.2.2 Radio frequency function

The main characteristics of the RF products are as follows:

- Support WCDMA/HSDPA/HSUPA900(850)/2100(1900)MHz；
- SupportGSM/GPRS/EDGE 850/900/1800/1900 MHz；
- The operating frequency range of the transmitter is shown in table 2-2.

Table 2-2 working frequency band

Working band	Upstream band（Uplink）	Downlink frequency band（Downlink）
UMTS850	824 MHz — 849 MHz	869 MHz — 894 MHz
UMTS900	890 MHz — 915MHz	925 MHz — 960 MHz
UMTS1900	1850 MHz — 1910 MHz	1930 MHz — 1990 MHz
UMTS2100	1920 MHz — 1980 MHz	2110 MHz — 2170 MHz
GSM850	824 MHz — 849MHz	869 MHz — 894 MHz

GSM900	890 MHz — 915MHz	925 MHz — 960MHz
GSM1800	1710 MHz — 1785MHz	1805 MHz — 1880MHz
GSM1900	1850 MHz — 1910MHz	1930 MHz — 1990MHz
CDMA BC0	869～894 MHz	824 ～849 MHz
TD-SCDMA B34	2010～2025 MHz	2010～2025 MHz
TD-SCDMA B39	1880～1920 MHz	1880～1920 MHz
TDD_LTE B38	2570 MHz~2620 MHz	2570 MHz~2620 MHz
TDD_LTE B39	1880 MHz~1920 MHz	1880 MHz~1920 MHz
TDD_LTE B40	2300 MHz~2400 MHz	2300 MHz~2400 MHz
TDD_LTE B41	2555～2655 MHz	2555～2655 MHz
FDD_LTE B1	1920 MHz~1980 MHz	2110 MHz~2170 MHz
FDD_LTE B3	1710 MHz~1785 MHz	1805 MHz~1880 MHz
FDD_LTE B7	2500 MHz~2570 MHz	2620 MHz~2690 MHz
FDD_LTE B8	880 MHz~915 MHz	925 MHz~960 MHz
FDD_LTE B20	832 MHz~862 MHz	791 MHz~821 MHz
GPS L1 BAND		1574.4 ～1576.44 MHz
GLONASS		1598 ～1606 MHz
BEIDOU B1		1559.05～1563.14 MHz

Table 2-3 Conducted transmission power

Frequency	Power Max.	PowerMin.
UMTS850	24dBm +1/-3dB	<-50dBm
UMTS900	24dBm +1/-3dB	<-50dBm
UMTS1900	24dBm +1/-3dB	<-50dBm
UMTS2100	24dBm +1/-3dB	<-50dBm
GSM850	33dBm ±2dB	5dBm ± 5dB
GSM900	33dBm ±2dB	5dBm ± 5dB
DCS1800	30dBm ±2dB	0dBm ± 5dB
PCS1900	30dBm ±2dB	0dBm ± 5dB
GSM850(8-PSK)	27dBm ±3dB	5dBm ± 5dB
GSM900(8-PSK)	27dBm ±3dB	5dBm ± 5dB
DCS1800(8-PSK)	26dBm +3/-4dB	0dBm ± 5dB
PCS1900(8-PSK)	26dBm +3/-4dB	0dBm ± 5dB

CDMA BC0	24dBm +1/-3dB	<-50dBm
CDMA BC1	24dBm +1/-3dB	<-50dBm
TD-SCDMA B34	24dBm +1/-3dB	<-50dBm
TD-SCDMA B39	24dBm +1/-3dB	<-50dBm
TDD_LTE B38	23dBm +/-2.7dB	<-40dBm
TDD_LTE B39	23dBm +/-2.7dB	<-40dBm
TDD_LTE B40	23dBm +/-2.7dB	<-40dBm
TDD_LTE B41	23dBm +/-2.7dB	<-40dBm
FDD_LTE B1	23dBm +/-2.7dB	<-40dBm
FDD_LTE B3	23dBm +/-2.7dB	<-40dBm
FDD_LTE B7	23dBm +/-2.7dB	<-40dBm
FDD_LTE B8	23dBm +/-2.7dB	<-40dBm
FDD_LTE B20	23dBm +/-2.7dB	<-40dBm

3 Interface description

3.1 Pin definition

3.1.1 Pin I/O parameter definition

The I/O parameter definition of the product is shown in table 3-1.

Table 3-1 I/O parameter definitions

Pin attribute symbol	Description
AI	Analog signal input pin
AO	Analog signal output pin
B	Bidirectional digital with CMOS input
DI	Digital signal input pin
DO	Digital signal output pin
H	High-voltage tolerant
Z	High-impedance output
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters andis a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pulldown with programmable options following the colon (:) PU: nppdkp = default pullup with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pullup device
PD	Contains an internal pulldown device
P1	EBI Pad group 1 (EBI for LPDDR2/LPDDR3 memory); tied to VDD_P1 pins (1.2 V only)
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (1.80 V or 2.95 V)
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.80 V only)
P4	Pad group 4 (UIM3); tied to VDD_P4 pins (1.80 V or 2.95 V)
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.80 V or 2.95 V)
P6	Pad group 6 (UIM2); tied to VDD_P6 pins (1.80 V or 2.95 V)

P7	Pad group 7 (SDC1); tied to VDD_P7 pins (1.80 V)
aVdd	Internally generated 1.875 V (typical) infrastructure supply for analog circuits
dVdd	Internally generated 1.8 V (typical) infrastructure supply for digital circuits
PU	Pin Internal pull up
PD	Pin Internal pull down
CSI	Supply voltage for MIPI_CSI circuits; tied to VDD_MIPI (1.2 V only)
DSI	Supply voltage for MIPI_DSI circuits; tied to VDD_MIPI (1.2 V only)
GND	Ground
PI	External power input

3.1.2 Pin configuration diagram

The product interface pin sequence is defined as the following Figure 3-1:：

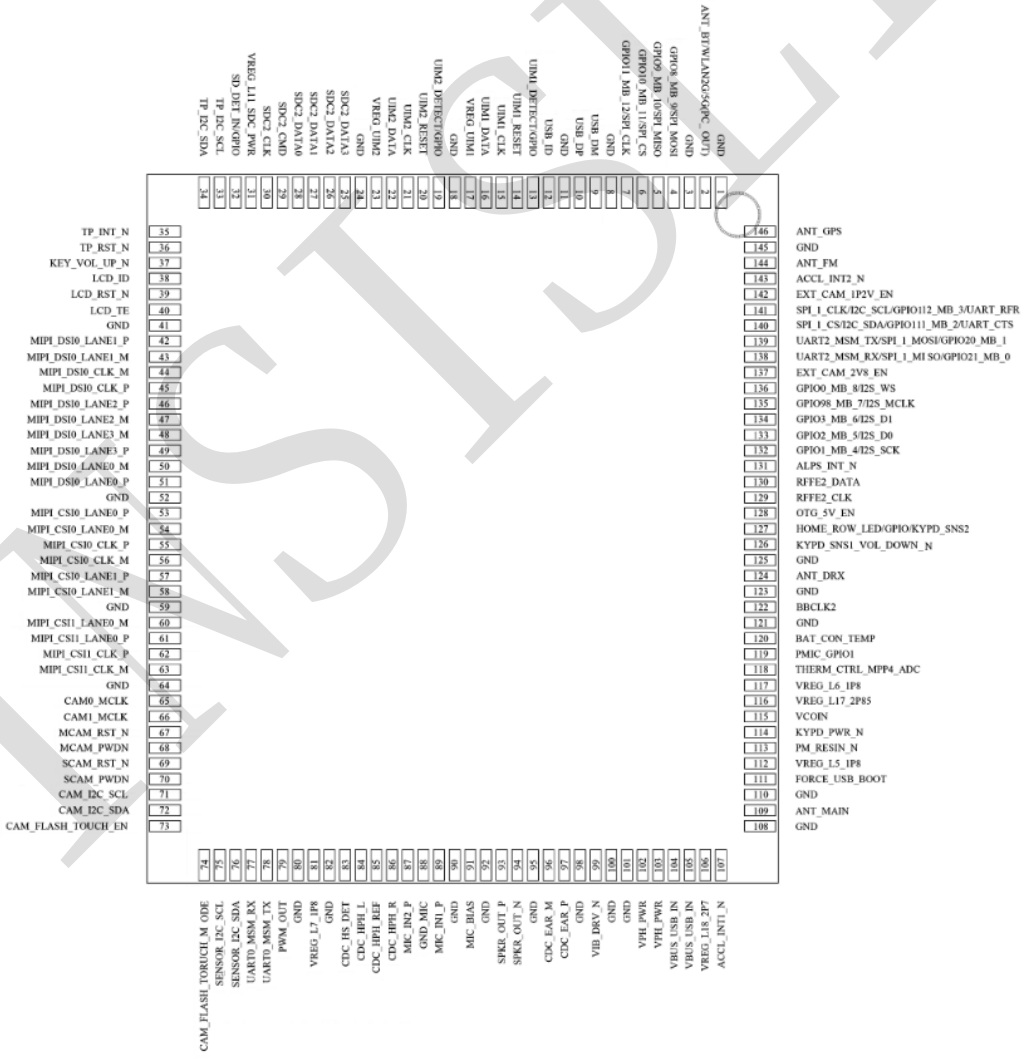


Figure 3-1 pin configuration diagram (positive view)

3.1.3 Pin description

Table 3-2 interface definition description:

Pin number	Module signal definition	Input / output	Pin voltage	Pin description
1	GND	--	--	Ground
2	ANT_BT/WLAN2G/5G(PC_OUT)	--	--	Antenna
3	GND	--	--	Ground
4	GPIO8_MB_9/SPI_MOSI	B	P3	GPIO8 /SPI_ Master Output/Slave Input
5	GPIO9_MB_10/SPI_MISO	B	P3	GPIO9/SPI_ Master Input/Slave Output
6	GPIO10_MB_11/SPI_CS	B	P3	GPIO10/SPI_ Chip select
7	GPIO11_MB_12/SPI_CLK	B	P3	GPIO11/SPI_Clock
8	GND	--	--	Ground
9	USB_DM	AI/AO	--	USB HS data minus
10	USB_DP	AI/AO		USB HS data plus
11	GND	--	--	Ground
12	USB_ID	AI	--	USB HS ID
13	UIM1_DETECT/GPIO	DI	P3	UIM1 presence detection
14	UIM1_RESET	DO	P5	UIM1 reset
15	UIM1_CLK	DO	P5	UIM1 clock
16	UIM1_DATA	B	P5	UIM1 data
17	VREG_UIM1	P	P5	UIM1 Power
18	GND	--	--	Ground
19	UIM2_DETECT/GPIO	DI	P3	UIM2 presence detection
20	UIM2_RESET	DO	P6	UIM2 reset
21	UIM2_CLK	DO	P6	UIM2 clock
22	UIM2_DATA	B	P6	UIM2 data
23	VREG_UIM2	P	P6	UIM2 Power
24	GND	--	--	Ground
25	SDC2_DATA3	BH-PD:nppukp	P2	Secure digital controller 2 data bit 3
26	SDC2_DATA2	BH-PD:nppukp	P2	Secure digital controller 2 data bit 2
27	SDC2_DATA1	BH-PD:nppukp	P2	Secure digital controller 2 data bit 1

28	SDC2_DATA0	BH-PD:nppukp	P2	Secure digital controller 2 data bit 0
29	SDC2_CMD	BH-PD:nppukp	P2	Secure digital controller 2 command
30	SDC2_CLK	BH-NP:pdpukp	P2	Secure digital controller 2 clock
31	VREG_L11_SDC_PWR	PO	--	SDC Power
32	SD_DET_IN/GPIO	DO	P3	SD Detect
33	TP_I2C_SCL	B	P3	TPI2CSCL
34	TP_I2C_SDA	B	P3	TPI2CSDA
35	TP_INT_N	B	P3	TPInterruptnegative input
36	TP_RST_N	B	P3	TPResetnegative input
37	KEY_VOL_UP_N	B-PD:nppukp DI	P3	Volume Key UP
38	LCD_ID	B	P3	LCD_ID
39	LCD_RST_N	B	P3	LCD resetnegative input
40	LCD_TE	B	P3	LCD_TE
41	GND	--	--	Ground
42	MIPI_DSI0_LANE1_P	AI, AO	DSI	MIPI display serial interface 0 lane 1 – pos
43	MIPI_DSI0_LANE1_M	AI, AO	DSI	MIPI display serial interface 0 lane 1 – neg
44	MIPI_DSI0_CLK_M	AO	DSI	MIPI display serial interface 0 clock – neg
45	MIPI_DSI0_CLK_P	AO	DSI	MIPI display serial interface 0 clock – pos
46	MIPI_DSI0_LANE2_P	AI, AO	DSI	MIPI display serial interface 0 lane 2 – pos
47	MIPI_DSI0_LANE2_M	AI, AO	DSI	MIPI display serial interface 0 lane 2– neg
48	MIPI_DSI0_LANE3_M	AI, AO	DSI	MIPI display serial interface 0 lane 3 – neg
49	MIPI_DSI0_LANE3_P	AI, AO	DSI	MIPI display serial interface 0 lane3 – pos
50	MIPI_DSI0_LANE0_M	AI, AO	DSI	MIPI display serial interface 0 lane 0– neg
51	MIPI_DSI0_LANE0_P	AI, AO	DSI	MIPI display serial interface 0 lane 0 – pos
52	GND	--	--	Ground
53	MIPI_CSI0_LANE0_P	AI, AO	CSI	MIPI camera serial interface lane 0 – pos
54	MIPI_CSI0_LANE0_M	AI, AO	CSI	MIPI camera serial interface lane 0 – neg
55	MIPI_CSI0_CLK_P	AI, AO	CSI	Camera serial interface clock – pos
56	MIPI_CSI0_CLK_M	AI, AO	CSI	Camera serial interface clock – neg
57	MIPI_CSI0_LANE1_P	AI, AO	CSI	MIPI camera serial interface lane 1 – pos
58	MIPI_CSI0_LANE1_M	AI, AO	CSI	MIPI camera serial interface lane 1 – neg
59	GND	--	--	Ground

60	MIPI_CSI1_LANE0_M	AI, AO	CSI	MIPI camera serial interface lane 3– neg
61	MIPI_CSI1_LANE0_P	AI, AO	CSI	MIPI camera serial interface lane 3– pos
62	MIPI_CSI1_CLK_P	AI, AO	CSI	Camera serial interface clock – pos
63	MIPI_CSI1_CLK_M	AI, AO	CSI	Camera serial interface clock – neg
64	GND	--	--	Ground
65	CAM0_MCLK	DO	P3	Camera master clock 0
66	CAM1_MCLK	DO	P3	Camera master clock 1
67	MCAM_RST_N	DO	P3	Camera 0 reset
68	MCAM_PWDN	DO	P3	Camera 0 standby
69	SCAM_RST_N	DO	P3	Camera 1 reset
70	SCAM_PWDN	DI	P3	Camera 1 standby
71	CAM_I2C_SCL	B-PD:nppukp	P3	CAMI2CSCL
72	CAM_I2C_SDA	B-PD:nppukp	P3	CAMI2CSDA
73	CAM_FLASH_TOUCH_EN	DO	P3	CAM_FLASH_TOUCH_EN
74	CAM_FLASH_TORUCH_MODE	DO	P3	CAM_FLASH_TORUCH_MODE
75	SENSOR_I2C_SCL	B	P3	SENSOR_I2C_SCL
76	SENSOR_I2C_SDA	B	P3	SENSOR_I2C_SDA
77	UART0_MSM_RX	B	P3	UART0 RX
78	UART0_MSM_TX	B	P3	UART0 TX
79	PWM_OUT	--	--	PWM_OUT
80	GND	--	--	Ground
81	VREG_L7_1P8	--	--	VREG_L7_1P8
82	GND	--	--	Ground
83	CDC_HS_DET	AI	--	Headset detection
84	CDC_HPH_L	AO	--	Headphone output, left channel
85	CDC_HPH_REF	AI	--	Headphone ground reference
86	CDC_HPH_R	AO	--	Headphone output, right channel
87	MIC_IN2_P	AI	--	Microphone input 2
88	GND_MIC	GND	--	Microphone bias filter ground
89	MIC_IN1_P	AI	--	Microphone input 1
90	GND	--	--	Ground
91	MIC_BIAS	--	--	MIC_BIAS

92	GND	--	--	Ground
93	SPKR_OUT_P	AO	--	Class-D speaker driver output, plus
94	SPKR_OUT_N	AO	--	Class-D speaker driver output, minus
95	GND	--	--	Ground
96	CDC_EAR_M	AO	--	Earpiece output, minus
97	CDC_EAR_P	AO	--	Earpiece output, plus
98	GND	--	--	Ground
99	VIB_DRV_N	PO	--	Vibration motor driver output control
100	GND	--	--	Ground
101	GND	--	--	Ground
102	VPH_PWR	PI	--	External power input
103	VPH_PWR	PI	--	External power input
104	VBUS_USB_IN	PI	--	Input power from USB source
105	VBUS_USB_IN	PI		Input power from USB source
106	VREG_L18_2P7	PO	--	VREG_L18_2P7
Pin number	Module signal definition	Input/output	Pin voltage	Pipe pin
107	ACCL_INT1_N	DI	P3	ACCL_INT1_N
108	GND	--	--	Ground
109	ANT_MAIN	--	--	Main Antenna
110	GND	--	--	Ground
111	FORCE_USB_BOOT	DO	P3	FORCE_USB_BOOT
112	VREG_L5_1P8	--	--	VREG_L5_1P8
113	PM_RESIN_N	DI	--	PMIC reset input
114	KYPD_PWR_N	DI	--	KYPD_PWR_N
115	VCOIN	AI/AO	--	Coin cell-battery or backup-battery charger supply and input.
116	VREG_L17_2P85	PO	--	VREG_L17_2P85
117	VREG_L6_1P8	PO	--	VREG_L6_1P8
118	THERM_CTRL_MPP4_ADC	DI/DO/AO	--	Configurable MPP
119	PMIC_GPIO1	DI/DO	--	PMIC_GPIO1
120	BAT_CON_TEMP	--	--	BAT_CON_TEMP
121	GND	--	--	Ground
122	BBCLK2	DO	--	Buffered baseband (low-power) XO clock 2

123	GND	--	--	Ground
124	ANT_DRX	--	--	ANT_DRX
125	GND	--	--	Ground
126	KYPD_SNS1_VOL_DOWN_N	B	P3	KYPD_SNS1_VOL_DOWN_N
127	HOME_ROW_LED/GPIO/KYPD_SNS2	B	P3	HOME_ROW_LED/GPIO/KYPD_SNS2
128	OTG_5V_EN	DO	P3	OTG_5V_EN
129	RFFE2_CLK	DI	P3	RFFE2_CLK
130	RFFE2_DATA	B	P3	RFFE2_DATA
131	ALPS_INT_N	B	P3	ALPS_INT_N
132	GPIO1_MB_4/I2S_SCK	B	P3	GPIO1_MB_4/I2S_SCK
133	GPIO2_MB_5/I2S_D0	B	P3	GPIO2_MB_5/I2S_D0
134	GPIO3_MB_6/I2S_D1	B	P3	GPIO3_MB_6/I2S_D1
135	GPIO98_MB_7/I2S_MCLK	DO-Z	P3	GPIO98_MB_7/I2S_MCLK
136	GPIO0_MB_8/I2S_WS	B	P3	GPIO0_MB_8/I2S_WS
137	EXT_CAM_2V8_EN	B	P3	EXT_CAM_2V8_EN
138	UART2_MSM_RX/SPI_1_MISO/GPIO21_MB_0	B	P3	UART2_MSM_RX/SPI_1_MISO/GPIO21_MB_0
139	UART2_MSM_TX/SPI_1_MOSI/GPIO20_MB_1	B	P4	UART2_MSM_TX/SPI_1_MOSI/GPIO20_MB_1
140	SPI_1_CS/I2C_SDA/GPIO111_MB_2/UART_CTS	B	P3	SPI_1_CS/I2C_SDA/GPIO111_MB_2/UART_CTS
141	SPI_1_CLK/I2C_SCL/GPIO112_MB_3/UART_RFR	B	P3	SPI_1_CLK/I2C_SCL/GPIO112_MB_3/UART_RFR
142	EXT_CAM_1P2V_EN	B	P3	EXT_CAM_1P2V_EN
143	ACCL_INT2_N	DO	P3	ACCL_INT2_N
144	ANT_FM	--	--	FM Antenna
145	GND	--	--	Ground
146	ANT_GPS	--	--	GPS Antenna

Note：1.P1 ~P7 is the power supply signal level set 1~7.

3.2 work Condition

Table **错误！文档中没有指定样式的文字。**-3 Module working condition:

Signal	Description	Minimum	Typical	Maximum	Unit
VBAT	Module main power supply	3.4	3.8	4.2	V
VDD_P1	Power for pad group 1	1.15	1.20	1.25	V
VDD_P2	Power for pad group 2				
	SDC2 pads low voltage	1.67	1.8	2.95	V
	SDC2 pads high voltage	2.75	1.93	3.04	V
VDD_P3	Power for pad group 3	1.67	1.8	1.93	V
VDD_P4	Power for pad group 4				
	UIM3 pads low voltage	1.67	1.8	2.95	V
	UIM3 pads high voltage	2.75	1.93	3.04	V
VDD_P5	Power for pad group 5				
	UIM1 pads low voltage	1.67	1.8	2.95	V
	UIM1 pads high voltage	2.75	1.93	3.04	V
VDD_P6	Power for pad group 6				
	UIM1 pads low voltage	1.67	1.8	2.95	V
	UIM1 pads high voltage	2.75	1.93	3.04	V
VDD_P7	Power for pad group 7	1.67	1.8	1.93	V

3.3 Interface electrical level Characteristic

3.3.1 Digital level signal characteristic

Table **错误！文档中没有指定样式的文字。**-4digital signal difference in degree electrical level scope

Symbol	Description	Minimum	Maximum	Unit
VIH	Input voltage high level	0.65*VDD_Px	-	V
VIL	Input voltage low level	-	0.35* VDD_Px	V
VOH	Output voltage high level	VDD_Px-0.45		V
VOL	Output voltage low level	0	0.45	V

Note：1. Typical voltage values are expressed in this product P3,

2. The design of the external circuit interface voltage must be matched with the pin voltage of the product.

3.4 Power supply interface

3.4.1 Power supply pin description

Pin number：102/103 pin is VBAT signal，3.8V positive signal for power supply.

Pin number：1/2/8/11/18/24/41/52/59/64/80/82/90/92/95/98/100/101/108/110/121/123/125/145is a GND signal.

This product's power and signal ground, the need to fully connect to the ground plane of the system board.GND signal connection is not complete will have an impact on the performance of the product.

Table **错误！文档中没有指定样式的文字。**-2 Definition and description of power supply

Pin number	Protocol signal name	Signal definition	current characteristic（V）		
			Minimum value	Typical value	Maximal value
102,103	VBAT	source supply electricity Input	3.4	3.8	4.2
1,2,8,11,18,24,41,52,59.64,80,82,90,92,95,98.100,101,108,110,121,123,125,145	GND	GND	-	-	-
17	VREG_L14_UIM1	UIM1 power	-	1.8	-
23	VREG_L15_UIM2	UIM2 power	-	1.8/3.0	-
31	VREG_L11_SDC	TF Card Power			
106	VREG_L18_2P7	RF Power1			
112	VREG_L5_1P8				
116	VREG_L17_2P85				
117	VREG_L6_1P8				
147	GND	Fixed pad	-	-	-

3.4.2 Power supply requirements

The power supply input signal power supply range is proposed for 3.4~4.2V. In the network environment, the antenna will be maximum power emission. The peak current of the module under the 4G mode may reach the peak current of 1.8A. Power supply need to reach 2A, the average current to reach 0.9A above.

3.5 USIM card interface

3.5.1 Pin description

The baseband processor of the M1503 module is integrated with double USIM card interface, which is in line with the standard of 7816-2 ISO, and can be detected automatically by 3.0V and USIM's 1.8V card, and the USIM card interface signal is shown in table 3-6.

Table **错误！文档中没有指定样式的文字。**-3(U) Definition and description of SIM card:

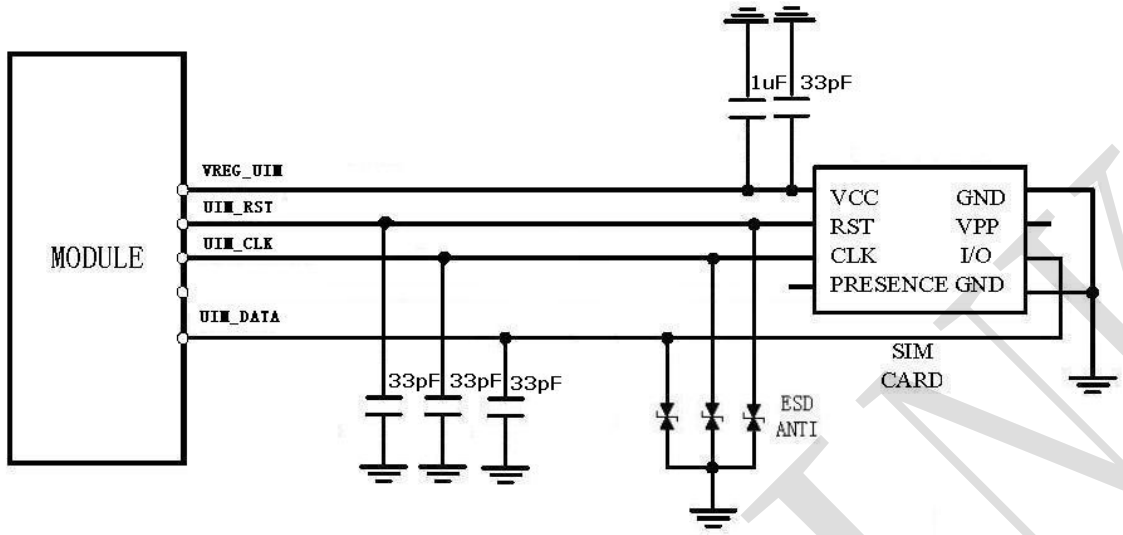
Pin number	Protocol signal name	Signal definition	Signal description
13	UIM1_DETECT/GPIO	UIM1 presence detection	UIM1 presence detection, input by module
14	UIM1_RESET	UIM1 reset pin	UIM1 reset，Output by module
15	UIM1_CLK	UIM1 clock pin	UIM1 clock，Output by module
16	UIM1_DATA	UIM1 data pin	UIM1 data，bidirectional signal
17	VREG_UIM1	UIM1 Power supply	UIM1 Power，Output by module
19	UIM2_DETECT/GPIO	UIM2 presence detection	UIM2 presence detection, input by module
20	UIM2_RESET	UIM2 reset pin	UIM2 reset，Output by module
21	UIM2_CLK	UIM2 clock pin	UIM2 clock，Output by module
22	UIM2_DATA	UIM2 data pin	UIM2 data，bidirectional signal
23	VREG_UIM2	UIM2 Power supply	UIM2 Power，Output by module

3.5.2 Electrical specification

USIM1 signal group (PIN number: 13,14,15,16,17.) and USIM2 signal group (PIN number: 19,20,21,22,23.).Each signal is defined in detail as shown in table 3-6. On the line near the USIM of the card holder, please pay attention to the need to increase the ESD protection device.

In order to meet the requirements of 3GPP TS 51.010-1 protocol and EMC certification, the proposed USIM card is arranged in close proximity to the position module USIM card interface, avoid due to go line is too long, resulting in serious waveform distortion, affecting the signal integrity of. USIM_CLK and USIM_DATA signal line is recommended to protect the GND and USIM_VCC in parallel between a 1uF and 33pF capacitor, USIM_CLK, USIM_RST, USIM_DATA and 33pF between the GND capacitor, filter out the interference of radio frequency signal.

3.5.3 USIM card interface application



Figure错误！文档中没有指定样式的文字。**-3 (U)** SIM card signal connection circuit

Note：USIM_DATA signal line on the pull of the resistor has been designed in the module, without the need to pull on the other.

3.6 USB2.0 Interface

3.6.1Pin description

This product has a high speed USB2.0 interface, support low-speed, full-speed and high-speed mode, the main processor (AP) and the module between the main data transmission through the USB interface.Table 3-8 gives the definition of the interface of USB

Table 3-7 USB Interface definition

Pin number	Signal name	I/O type	Direct characteristic（V）		
			Minimum value	Typical value	Maximal value
9	USB_DM	USB2.0 data signal D-	-	-	-
10	USB_DP	USB2.0 data signal D+	-	-	-

3.6.2 Electrical character

The USB interface of the module conforms to the USB2.0 specification and electrical characteristics.Supports low-speed, full-speed and high-speed three kinds of work mode, the main processor (AP) and the data exchange between the modules is completed by the USB interface.

3.6.3USBInterface application

USB bus is mainly used for data transmission, software upgrading, module testing.Work in the high-speed mode of the USB line, if you need ESD design, ESD protection device must meet the junction capacitance value <5pf, otherwise the larger junction capacitance will cause waveform distortion, the impact of bus communication. Differential impedance of differential data line in 90ohm + 10%.

3.7 I2SInterface

3.7.1 Pin description

This product has I2S interface, and this IO can use as GPIO.Table 3-8 gives the definition of the interface of I2S/GPIO.

Table 3-8I2S Interface definition

Pin number	Signal name	I/O type	Function description
132	GPIO1_MB_4/I2S_SCK	B	GPIO1_MB_4/I2S_SCK
133	GPIO2_MB_5/I2S_D0	B	GPIO2_MB_5/I2S_D0
134	GPIO3_MB_6/I2S_D1	B	GPIO3_MB_6/I2S_D1
135	GPIO98_MB_7/I2S_MCLK	DO-Z	GPIO98_MB_7/I2S_MCLK
136	GPIO0_MB_8/I2S_WS	B	GPIO0_MB_8/I2S_WS

3.8UART Interface

3.8.1 Pin description

M1503 module provides two way serial communication interface UART: Which the UART1 as a module M1503 debug port, for the 2 line UART interface;

UART0 as a complete non synchronous communication interface, the signal control of the standard modem handshake signal,In line with the RS-232 interface protocol, it also supports 4 serial bus interface or 2 wire serial bus interface mode,The module can communicate with the outside world through the UART interface and the AT instruction input.

These two groups of UART ports support programmable data width, programmable data stop bits, programmable parity bits, with independent TX and FIFOs RX (each 512 bytes),For maximum baud rate of normal application of UART (non-Bluetooth) 230400bps and 4Mbps high-speed baud rate is only supported in the Bluetooth 2.0 applications, the default baud rate to 115200bps. Pin signal definition as shown in table 3-9.

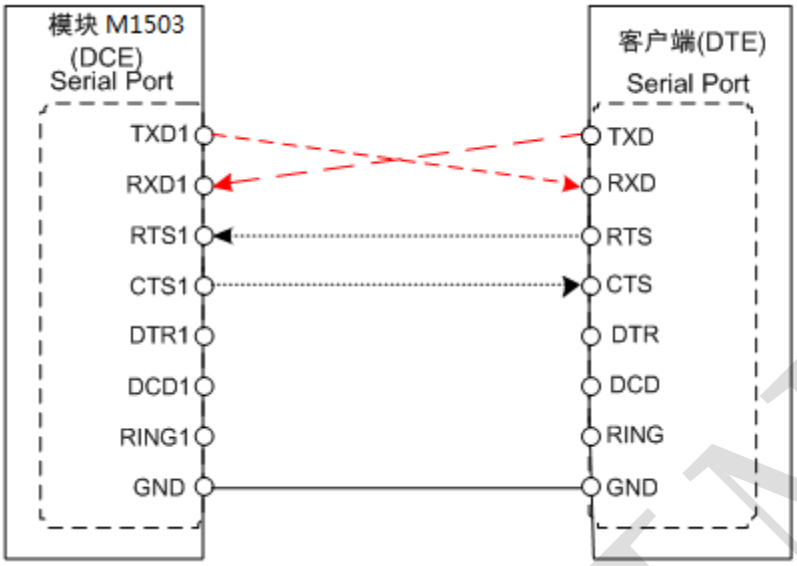
Table **错误！文档中没有指定样式的文字。**-4UART Signal definition

Pin number	Signal name	I/O type	Function description
77	UART0_MSM_RX	DI	UART0 RX
78	UART0_MSM_TX	DO	UART0 TX
138	UART2_MSM_RX/SPI_1_MISO/GPIO21_MB_0	B	UART2_MSM_RX/SPI_1_MISO/GPIO21_MB_0
139	UART2_MSM_TX/SPI_1_MOSI/GPIO20_MB_1	B	UART2_MSM_TX/SPI_1_MOSI/GPIO20_MB_1
140	SPI_1_CS/I2C_SDA/GPIO111_MB_2/UART_CTS	B	SPI_1_CS/I2C_SDA/GPIO111_MB_2/UART_CTS
141	SPI_1_CLK/I2C_SCL/GPIO112_MB_3/UART_RFR	B	SPI_1_CLK/I2C_SCL/GPIO112_MB_3/UART_RFR

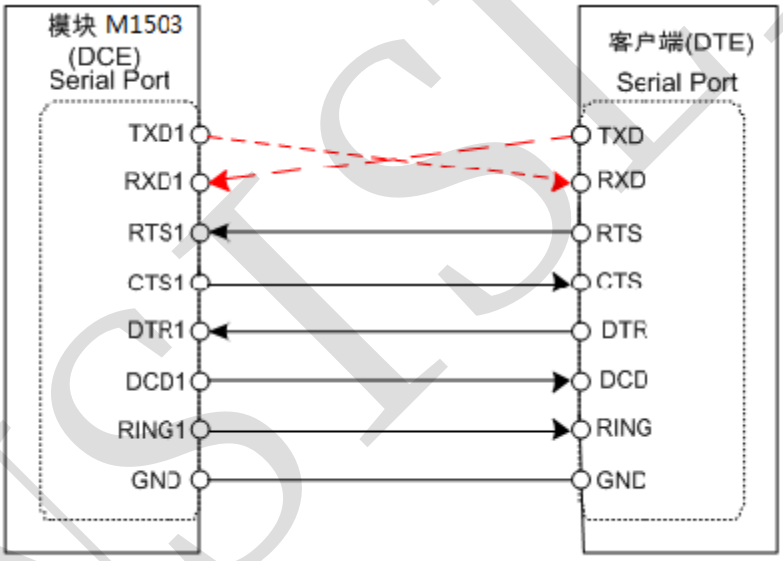
3.8.2 UARTInterface electrical properties

UART1in order to have a means to capture log in the software，We recommend that users keep the interface and test points.

UART2 if used in the module and application processor communication, and level in 1.8V matching, the connection mode is shown in Figure 3-3 and figure 3-4, complete RS232 model can be used, 4 line mode or 2 wire mode connection。Module interface level is 1.8V, if it does not match the AP interface level, it is recommended to increase the level of conversion circuit.



Figure错误！文档中没有指定样式的文字。-3Module serial port and AP application processor 4 line connection method



Figure错误！文档中没有指定样式的文字。-4Module serial port and AP application processor complete connection method

3.9 Open / shut down and reset interface

3.9.1Pin description

The product of the boot process is: pull the POWER_ON_OFF pin down to 8 seconds, and then the tube feet dangling or pull high, you can turn on;

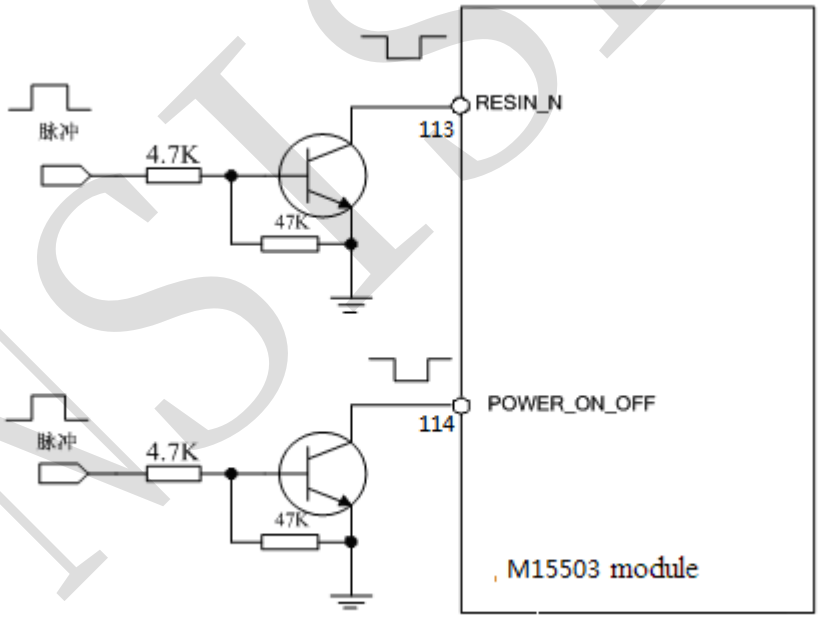
RESIN_N pin for the reset module，After pulling the RESIN_N pin to the low 200ms，And then put the tube foot floating or high，Can reset。After reset，Need to pull the POWER_ON_OFF pin down 3 seconds above，Can be reset boot。Interface definition as shown in Table 3-10:

Table **错误！文档中没有指定样式的文字。**-10Switch machine and reset button signal definition

Pin number	Signal name	I/O type	Function description
113	PM_RESIN_N	DI	PMIC reset input
114	KYPD_PWR_N	DI	Module switch machine key，pull up to dVdd

3.9.2Interface application

KYPD_PWR_N and PM_RESIN_Ncircuits can refer to the design circuit shown in Figure 3-5，The two input signals on the left of the diagram are respectively the reset and the input control signal of the power on the left.



Figure错误！文档中没有指定样式的文字。**-5** Boot / reset recommended circuit

3.10 Analog audio interface

3.10.1 Pin description

M1503 module provides analog audio interface, as the receiver and free voice channel voice channel, the voice channel and free speech channel pin definition such as 3-11 shown in table:

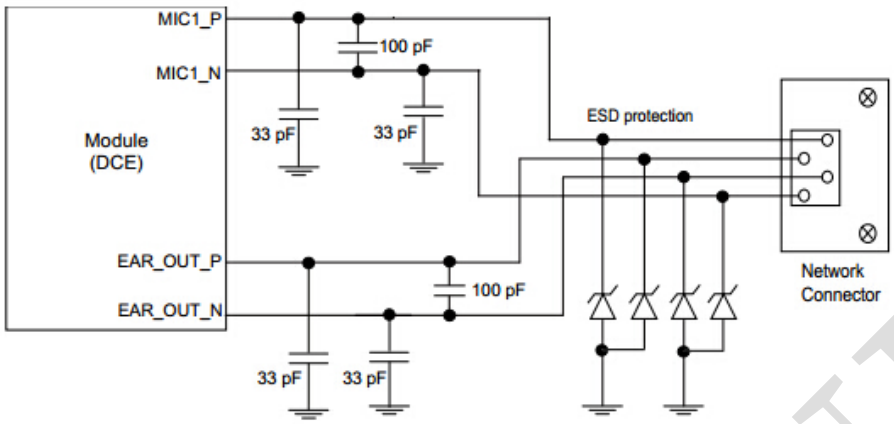
Table **错误！文档中没有指定样式的文字。**-1 The speech channel pin definition

Pin number	Signal name	I/O type	Function description
83	CDC_HS_DET	AI	Headset detection
84	CDC_HPH_L	AO	Headphone output, left channel
85	CDC_HPH_REF	AI	Headphone ground reference
86	CDC_HPH_R	AO	Headphone output, right channel
87	MIC_IN2_P	AI	Microphone input 2
88	GND_MIC	GND	Microphone bias filter ground
89	MIC_IN1_P	AI	Microphone input 1
90	GND	--	Ground
91	MIC_BIAS	--	MIC_BIAS
92	GND	--	Ground
93	SPKR_OUT_P	AO	Class-D speaker driver output, plus
94	SPKR_OUT_N	AO	Class-D speaker driver output, minus
95	GND	--	Ground
96	CDC_EAR_M	AO	Earpiece output, minus
97	CDC_EAR_P	AO	Earpiece output, plus

3.10.2 Interface application

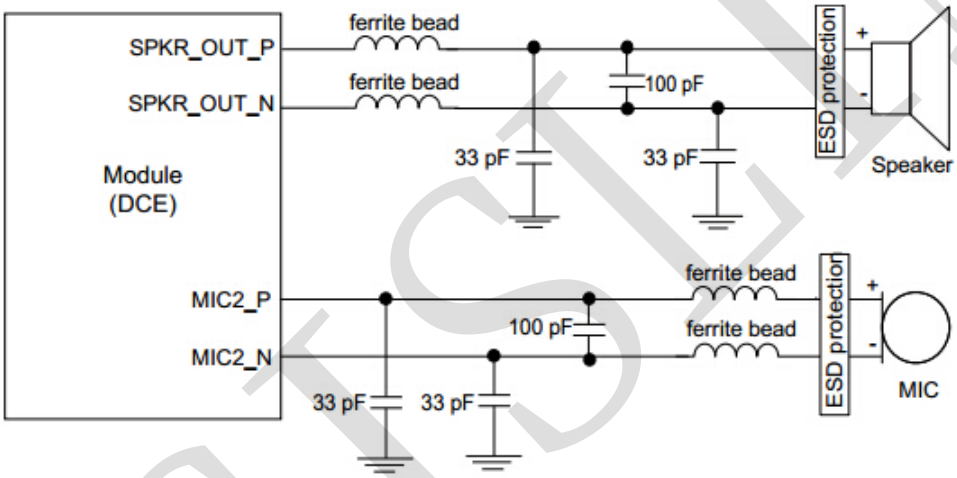
M1503 provides the handset voice channel and free voice channel into two independent channels, n the process of using the EAR_OUT collocation MIC1 pathway，Outside the SPK_OUT collocation MIC2 channel.

EAR_OUT can directly drive 32 ohm, the maximum output power is 50mW, You can also directly drive the Codec Line in AP interface to do the output of the module's voice signal，The corresponding module of the speech signal input selects the MIC1 pathway。Figure 3-6 is a schematic diagram of the receiver circuit to drive the users receiver。



Figure错误！文档中没有指定样式的文字。**-6**Schematic diagram of receiver circuit

SPK_OUTCan directly drive 8 Ohm's horn，The maximum output power is 1.5W。Figure 3-7 circuit diagram for driving 8 ohm Speaker.



Figure错误！文档中没有指定样式的文字。**-7**Schematic diagram of Speaker circuit

3.10.3Audio signal PCB

PCB Layout，EAR_OUT,MIC1,SPK_OUT,MIC2 Shall be carried out in strict accordance with the rules of differential layout，and need to protect the right and left.Among them,EAR_OUT, MIC1 and MIC2 signal can go on a single 6mil,SPK_OUT single 20MIL signal to go,The audio line must be far away from the RF radio frequency signal line, switching power supply or other high-speed digital signal.

Each audio signal line in close proximity to the audio connector or socket, suggestion and 33pf capacitor to prevent RF signal coupling leads to noise current and series magnetic beads and add the corresponding ESD protection devices.

3.11 Camera interface

3.11.1 Pin description

M1503 module provides two MIPI_CSIs camera interface, CSI0 is 2-lane CSI,CSI1 is a

1-line CSI.Pin definition such as 3-12 shown in table:

Table **错误！文档中没有指定样式的文字。**-52 The speech channel pin definition

Pin number	Signal name	I/O type	Function description
53	MIPI_CSI0_LANE0_P	AI, AO	MIPI camera serial interface lane 0 – pos
54	MIPI_CSI0_LANE0_M	AI, AO	MIPI camera serial interface lane 0 – neg
55	MIPI_CSI0_CLK_P	AI, AO	Camera serial interface clock – pos
56	MIPI_CSI0_CLK_M	AI, AO	Camera serial interface clock – neg
57	MIPI_CSI0_LANE1_P	AI, AO	MIPI camera serial interface lane 1 – pos
58	MIPI_CSI0_LANE1_M	AI, AO	MIPI camera serial interface lane 1 – neg
60	MIPI_CSI1_LANE0_M	AI, AO	MIPI camera serial interface lane 3– neg
61	MIPI_CSI1_LANE0_P	AI, AO	MIPI camera serial interface lane 3– pos
62	MIPI_CSI1_CLK_P	AI, AO	Camera serial interface clock – pos
63	MIPI_CSI1_CLK_M	AI, AO	Camera serial interface clock – neg
65	CAM0_MCLK	DO	Camera master clock 0
66	CAM1_MCLK	DO	Camera master clock 1
67	MCAM_RST_N	DO	Camera 0 reset
68	MCAM_PWDN	DO	Camera 0 standby
69	SCAM_RST_N	DO	Camera 1 reset
70	SCAM_PWDN	DI	Camera 1 standby
71	CAM_I2C_SCL	B-PD:nppukp	CAMI2CSCL
72	CAM_I2C_SDA	B-PD:nppukp	CAMI2CSDA
73	CAM_FLASH_TOUCH_EN	DO	CAM_FLASH_TOUCH_EN
74	CAM_FLASH_TORUCH_MODE	DO	CAM_FLASH_TORUCH_MODE

3.11.2Interface application

M1503 module provides two MIPI_CSIs camera interface, CSI0 is 2-lane CSI,CSI1 is a 1-line CSI.Figure3-8 is a schematic diagram of 2-lane CSI camera circuit to drive the user of camera:

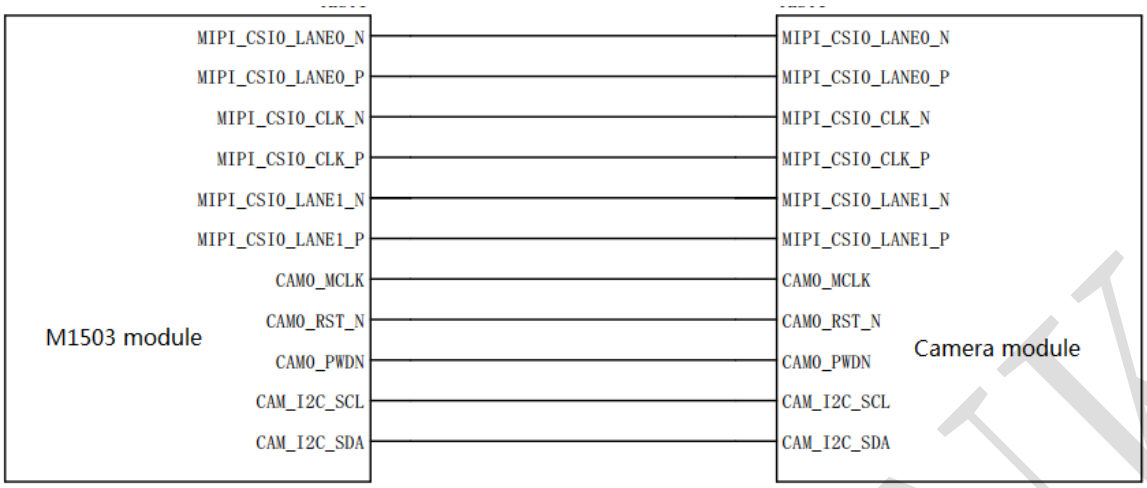


Figure 错误！文档中没有指定样式的文字。**-8**Schematic diagram of camera circuit

Figure3-9 is a schematic diagram of 1-lane CSI camera circuit to drive the user of camera:

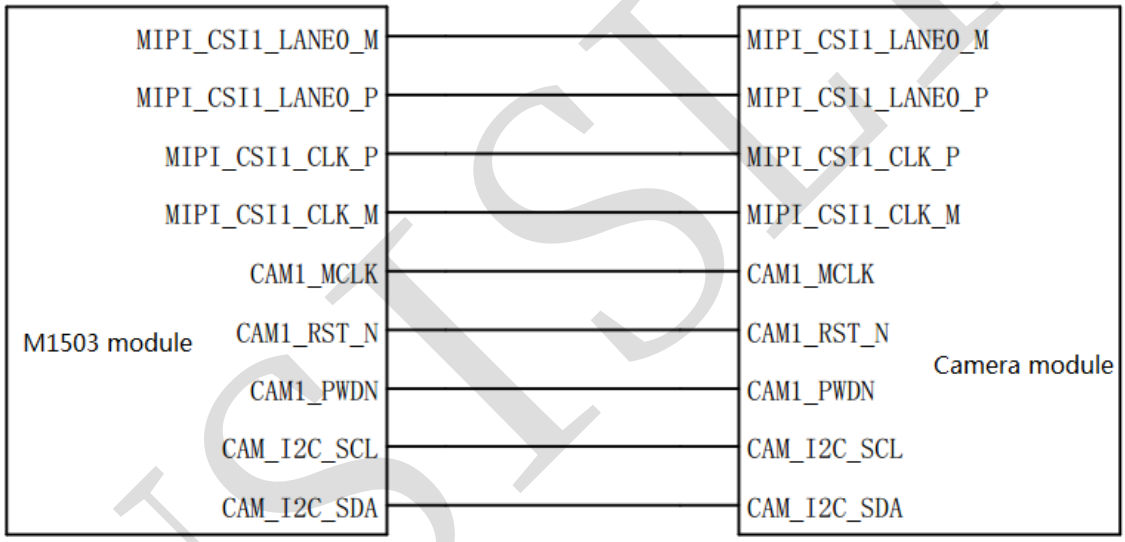


Figure 错误！文档中没有指定样式的文字。**-4**Schematic diagram of camera circuit

3.12LCD and Touch interface

3.12.1Pin description

M1503 module provides a 4-lane MIPI_DSI LCD interface, and I2C Touch control interface,Pin definition such as 3-13 shown in table:

Table **错误！文档中没有指定样式的文字。**-63 The speech channel pin definition

Pin number	Signal name	I/O type	Function description
33	TP_I2C_SCL	B	TPI2CSCL
34	TP_I2C_SDA	B	TPI2CSDA

35	TP_INT_N	B	TP Interrupt negative input
36	TP_RST_N	B	TP Reset negative input
38	LCD_ID	B	LCD_ID
39	LCD_RST_N	B	LCD resetnegative input
40	LCD_TE	B	LCD_TE
42	MIPI_DSI0_LANE1_P	AI, AO	MIPI display serial interface 0 lane 1 – pos
43	MIPI_DSI0_LANE1_M	AI, AO	MIPI display serial interface 0 lane 1 – neg
44	MIPI_DSI0_CLK_M	AO	MIPI display serial interface 0 clock – neg
45	MIPI_DSI0_CLK_P	AO	MIPI display serial interface 0 clock – pos
46	MIPI_DSI0_LANE2_P	AI, AO	MIPI display serial interface 0 lane 2 – pos
47	MIPI_DSI0_LANE2_M	AI, AO	MIPI display serial interface 0 lane 2– neg
48	MIPI_DSI0_LANE3_M	AI, AO	MIPI display serial interface 0 lane 3 – neg
49	MIPI_DSI0_LANE3_P	AI, AO	MIPI display serial interface 0 lane3 – pos
50	MIPI_DSI0_LANE0_M	AI, AO	MIPI display serial interface 0 lane 0– neg
51	MIPI_DSI0_LANE0_P	AI, AO	MIPI display serial interface 0 lane 0 – pos

3.12.2Interface application

M1503 module provides a 4-lane MIPI_DSI LCD interface,and I2C Touch control interface.

Figure 3-10 is a schematic diagram of Touch interface.

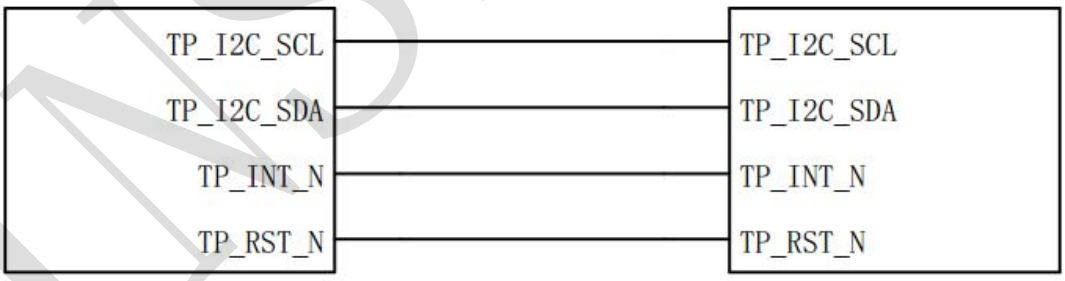


Figure 错误！文档中没有指定样式的文字。**-10**Schematic diagram of Touch

Figure 3-11 is a schematic diagram of 4-lane MIPI_DSI LCD interface .

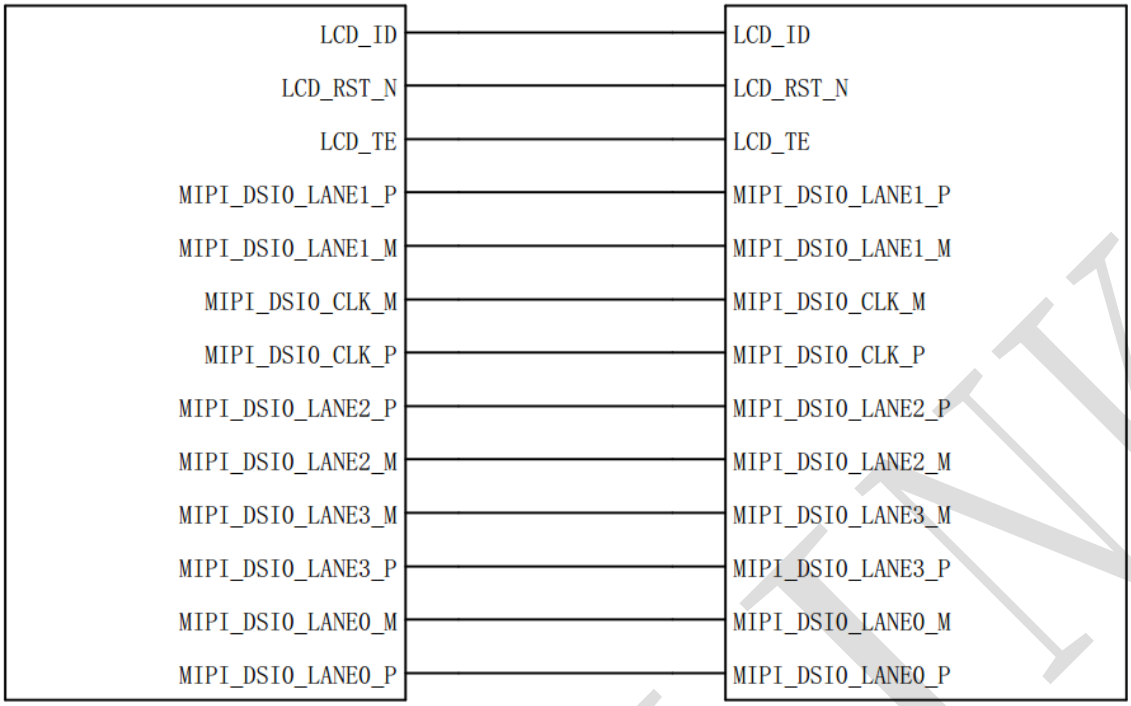


Figure 错误！文档中没有指定样式的文字。**-11**Schematic diagram of LCD

3.13 Antenna interface

3.13.1 Antenna signal Go line rule

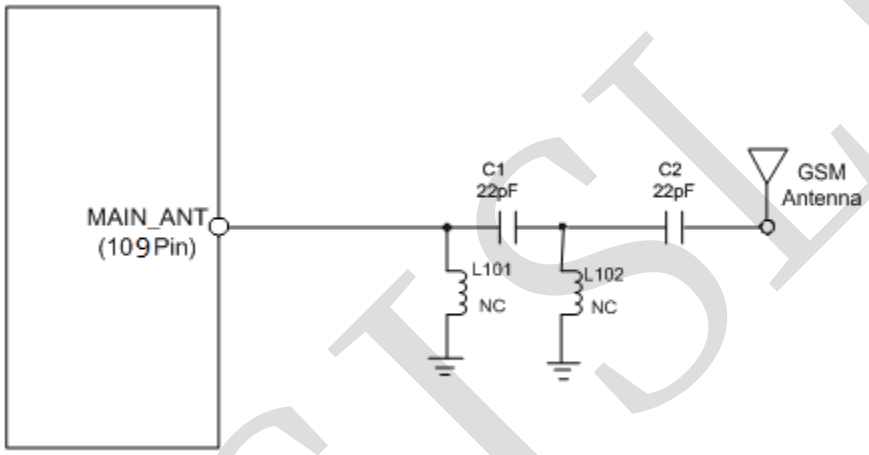
The M1503 module provides an antenna feed point on the LCC pad,Antenna signal wire can be directly pulled out from the pad，Matching via the antenna, type T or type circuit. Antenna feed point defined as shown in table 3-14:

Table **错误！文档中没有指定样式的文字。**-74 Antenna feed point pin definition

Pin number	Signal name	I/O type	Function description
109	MAIN_ANT	AI/AO	Antenna feed point

3.13.2Interface application

Antenna basic circuit design as shown in figure 3-12:



Figure错误！文档中没有指定样式的文字。**-12**Antenna feed point circuit

In layout design，Antenna RF transmission line must be guaranteed that the characteristic impedance of =50 ohm,This characteristic impedance is made from the substrate plate, Line width and off ground plane distance codetermine.

4 Product electrical characteristics

4.1 Power Supply Characteristic

4.1.1 Power Supply Voltage

The input voltage range of the product is 3.4V~4.2V DC, The typical value is 3.8V，As shown in table 4-1.

Table 4-1 input voltage

parameter	Minimum value	Typical value	Maximum value
input voltage	3.4V	3.8V	4.2V

4.1.2 Switch machine process

The starting process is divided into two kinds of situations: System for the first time and System operation process Re enable module. The same process in two cases，As shown in Figure 4-1.

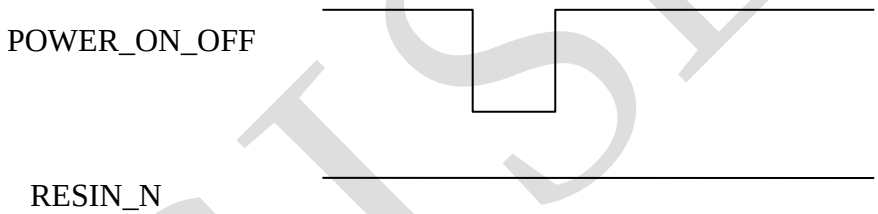


Figure 4-1 boot process

As shown in figure, Application processors need to control the formation of POWER_ON_OFF pulse，the pulse width should be in 8 seconds or so. Before the fall of POWER_ON_OFF，Module does not work, In an off state. When the module detects the falling edge of the POWER_ON_OFF, the boot is started, Enumeration of the USB interface after the initialization, application processor USB device file appears.

Shutdown process occurred in the whole system is turned off as well as the time to turn off the module in the running process.

4.1.3 Reset process

When the application processor needs to reset the module, Control RESIN_N reset signal generated by pulse, Pulse width need to be greater than 2ms, Recommended width 200ms.POWER_ON_OFF signal to remain high。

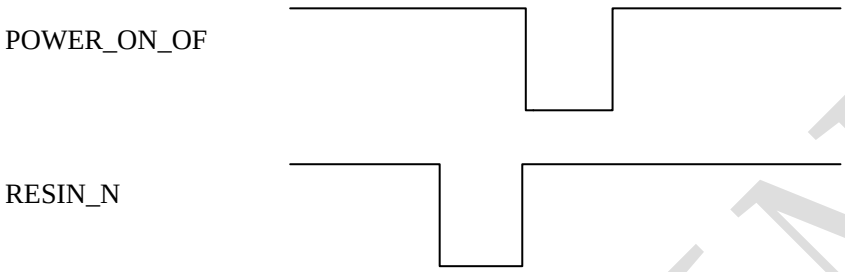


Figure 4-2 Module reset flow chart

When the RESIN_N signal is pulled high, POWER_ON_OFF signal to produce a lower pulse, the width of the pulse is the same as the starting process.

5 Design guidance

This chapter provides general guidance for design of this product, Users can refer to design guidance for design, make the product to achieve better performance.

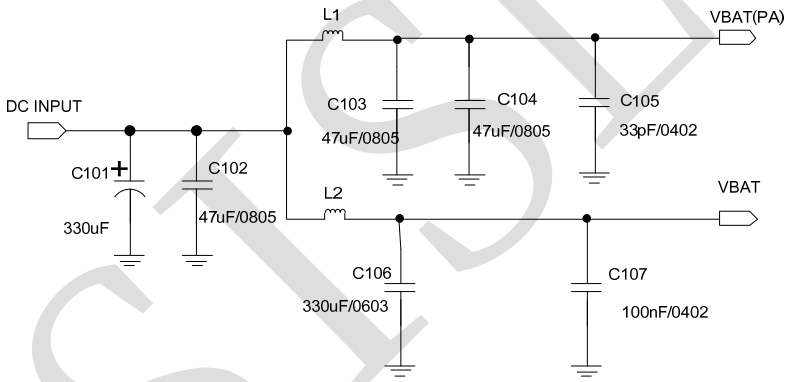
5.1 General design rules and requirements

Users in the design of the peripheral circuits of this product, first of all, we must ensure that the external power supply circuit can provide adequate power supply, and for high speed signal line USB request control 90ohm 10% differential impedance. For

general signal interface, require users in strict accordance with our requirements for design, meet interface signal level matching, to prevent the level of inconsistent damage module. This product has good RF index, the customer needs to design the main board side antenna circuit according to the requirement and make the corresponding impedance control, otherwise it will affect the radio frequency index.

5.2 Power supply Circuit design

The power supply capacity of the system board is required to reach 2A above VPH_PWR, meet peak current demand of module，And the average current of the power supply of the system should reach above 0.9A. System board side power supply line should be sufficient to ensure that line width, and Ground plane Form a good return, In addition in the power supply circuit design should increase the level of energy storage capacitor hundred micro method, Guarantee instantaneous power supply, and power supply ripple control in 100mV, Reference power supply circuit design 7-1 is shown.



Figure错误！文档中没有指定样式的文字。**-5**Reference for power supply circuit

5.3 RF circuit design

5.3.1 Initial antenna design note

- Pre project evaluation

The selection of the antenna position must first ensure that the antenna and the base station are kept in the horizontal direction, this produces the highest efficiency; Secondly, try to avoid placing the switch in the power supply or data line、Chip and other devices or chips that produce electromagnetic interference. At the same time, the position of the hand can be avoided, So as to prevent the human body to produce attenuation; But also to reduce the radiation and the structure of the realization of the need to take into account. So, At the beginning of the design need to structure, ID, circuit, antenna engineers together to evaluate the layout.

- Antenna placement Position suggestion

Antenna placement for notebook products: the ideal position is placed in the upper left or right of the LCD, this position is far from the motherboard, small electromagnetic interference，Two is considered to be far from the human body, SAR index easy to meet；The next better placement is the left or right side of LCD.Other products such as routers, e-books, etc.According to the characteristics of the product itself.

- Antenna occupancy space

Because different antenna manufacturers may adopt different antenna types, So, antenna reserved space is also different:3Gfive frequency main antenna：5mm（Thick）*12mm（Wide）*80mm（Long）。

- Motherboard Layout

Motherboard area has a strong interference, experimental results show that the module is placed in the disturbed area, resulting in poor performance. When the notebook design best to separate the module and the motherboard PCB, Instead of installing it on the motherboard. If it is not possible to make the separation, the module is far away from the chip and memory, power supply interface, data line interface, and other possible EMI modules and devices.

- Antenna matching circuit

If the module's radio frequency port and the antenna interface need to be transferred, the main board circuit design, The design of microstrip line or strip line between the module RF test base and the antenna interface between the microstrip line or the strip line by characteristic impedance 50 ohm, at the same time, reserved double L type matching circuit; If the antenna's RF connector can be directly stuck in the module's RF test base, can save the module of the RF port and the antenna interface between the transfer.

5.4 EMC and ESDDesign suggestion

Users should take full account of the EMC problem caused by signal integrity and power integrity in the design of the whole machine, In the module of the peripheral circuit layout, for power and signal lines, etc., to maintain the spacing of 2 times line width, Can effectively reduce the coupling between the signal, so that the signal has a clean, the return path. When the peripheral power supply circuit is designed, the decoupling capacitor should be placed close to the module power supply pin, High frequency high speed circuit and sensitive circuit should be far from the edge of PCB, and the layout of the layout as far as possible to reduce the interference between each other, and the sensitive signal is protected, The circuit or device that may interfere with the operation of the system board is designed.

This product is embedded in the system board side, design, need to pay attention to the ESD protection, The key input and output signal interface, such as (U) SIM card interface,

etc., need to be placed close to the protection of ESD devices, In addition to the motherboard side, the user is required to design the structure and PCB layout, ensure that the metal shield is fully grounded, and set up an unobstructed discharge passage for the electrostatic discharge.

5.5 PCB Pad design

We recommend that the user in the design of the main board of the package, in the middle of the 12 heat pad, according to the size of Figure5-2 in the design.The main antenna 0.3mm is proposed to be a fillet of radius, This is more conducive to the interference of the incoming and radio frequency signal.

Recommended PCB pads as shown in figure 5-2:

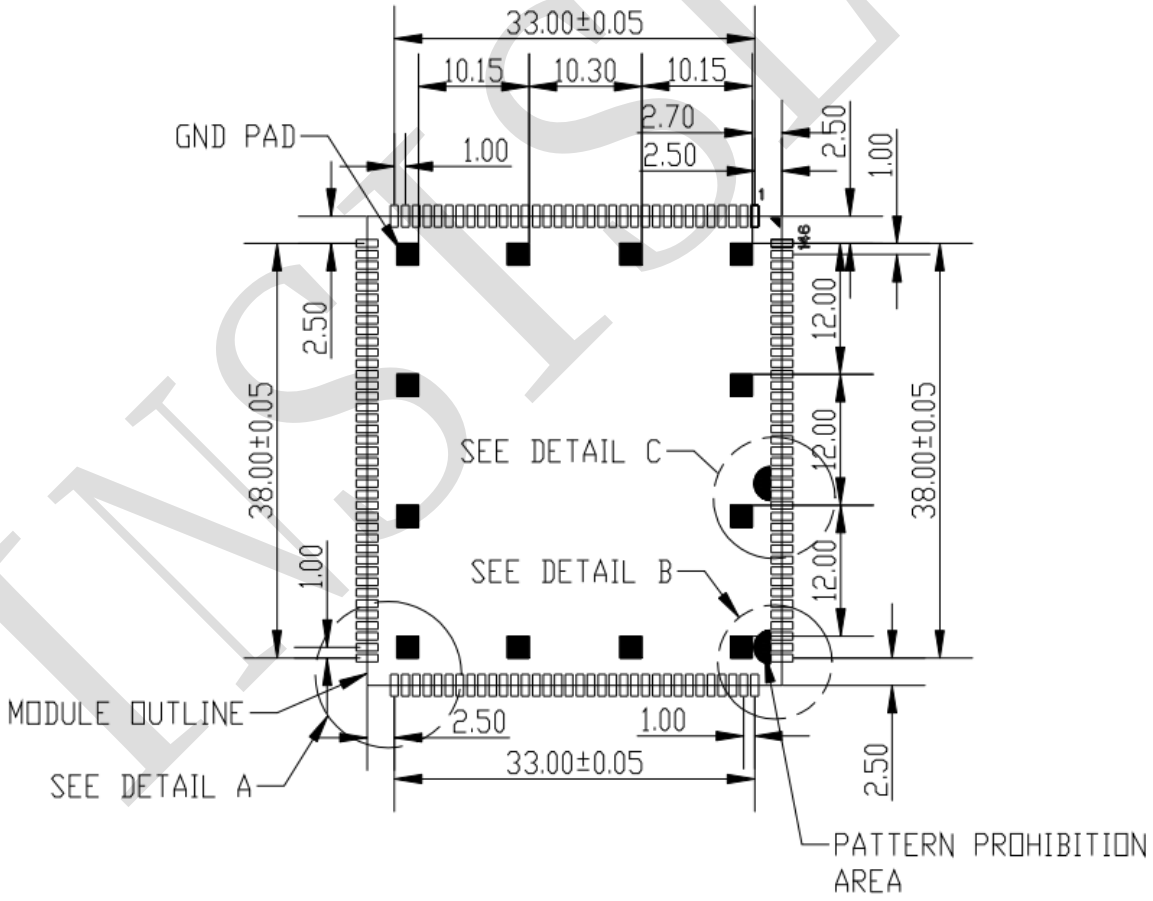


Figure 错误！文档中没有指定样式的文字。**-6**Recommended PCB pad

5.6 Thermal design suggestion

Module in the process of work itself will heat, it may also be influenced by other high temperature devices. The product design of the heat dissipation is considered, the bottom of the module is left with 30 heat pads, when connecting with the system board, please keep these ground heat welded plate ground well, this is a great help for heat conduction and heat balance，at the same time, the electrical performance of the whole machine is also very good.

Please note：

1）As far as possible to make this module products away from the switching power supply, high speed signal line, and the source of these disturbances to protect the line.

2）Antenna and cable and antenna coaxial cable at the same time do not come close to the source of these disturbances.

3）Don't let near the module such as CPU, Southbridge heat larger devices placed, temperature will affect the RF performance.

5.7 Product recommendation Upgrade plan

When the module is designed, we propose to connect the SD interface signal to the test point or the SD/micro-SD interface, in order to upgrade the use of firmware in the module.（Not realized）

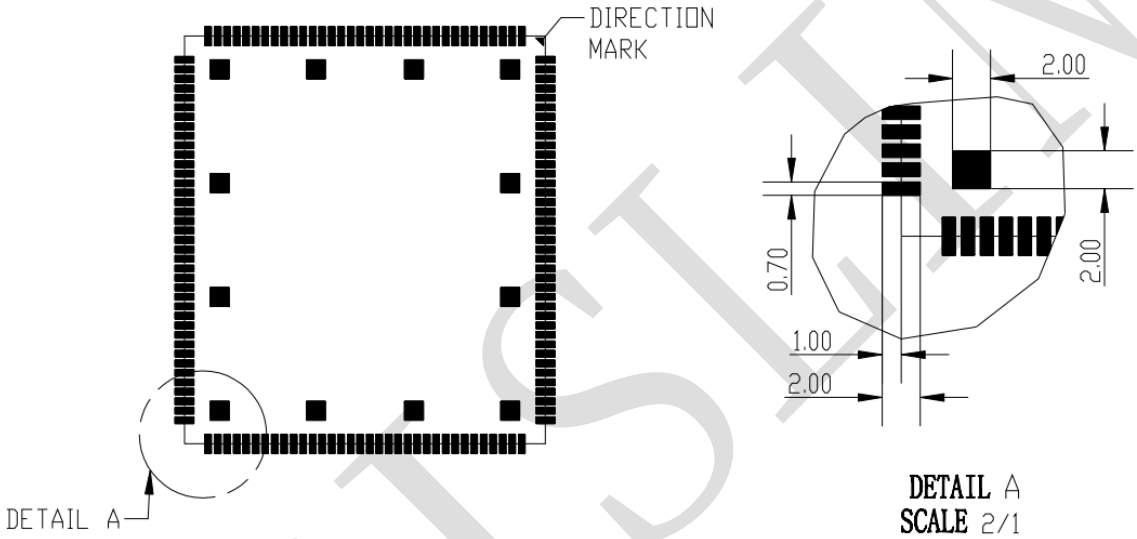
6 Production guidance

6.1. Steel net design

Steel mesh design need to pay attention:

1）At the bottom of the module pad thermal, can be reduced by way of steel mesh openings, reduce the risk of short circuit between the thermal and the module of the module Pin, have certain effect;

2）Module pad thermal welded steel mesh openings are recommended for reference. Figure 6-1 is recommended for steel mesh and size.



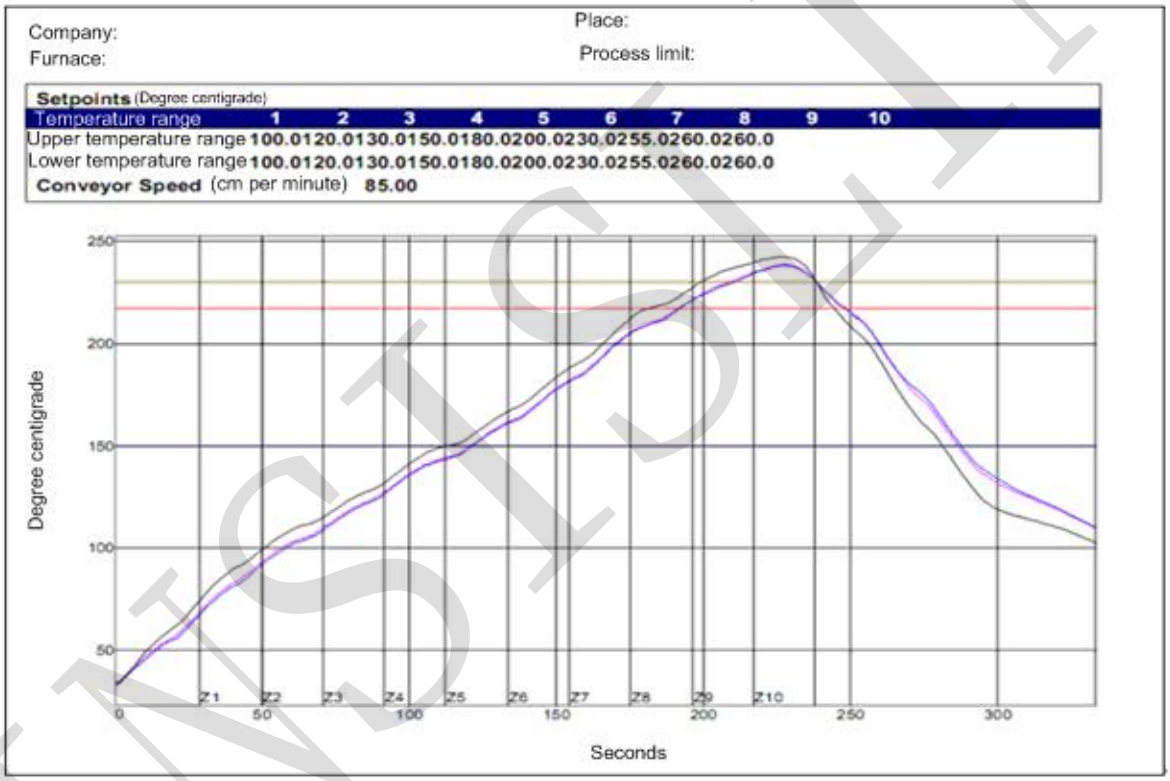
Figure错误！文档中没有指定样式的文字。**-7**Recommended pad steel mesh

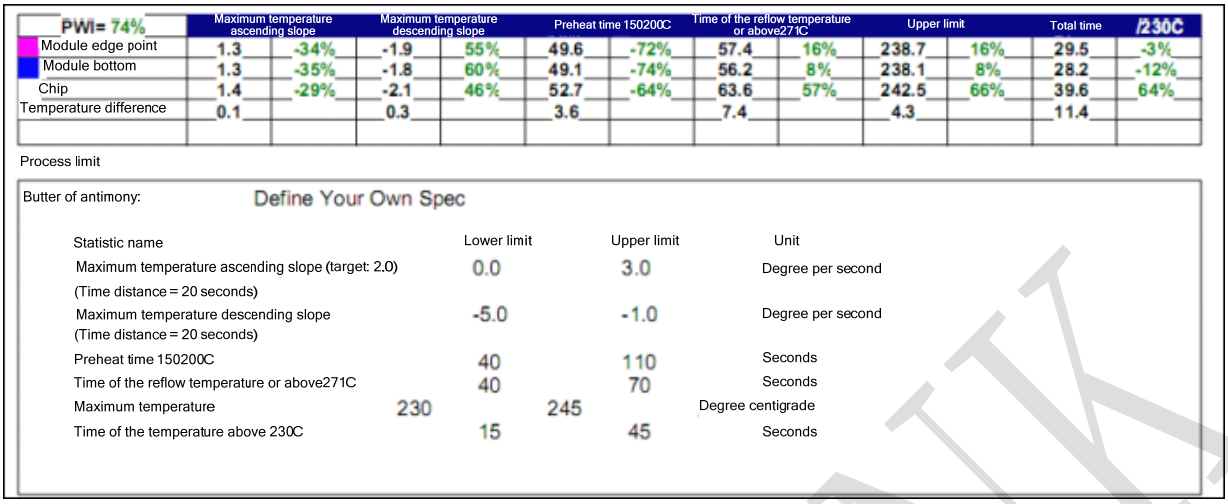
6.2. Temperature curve

The temperature curve of the welding quality and material status influence, please pay special attention. Temperature rise speed should not be too fast, from room temperature to 150, the temperature rise rate is less than 3s. At the same time in more than 217 degrees, please try to keep time no more than 70 seconds, at intermediate values of 55 seconds is appropriate. The thermal shock strength is too general will lead to part of the device failure, resulting in a decline in yield and maintenance difficulty. And please control the maximum temperature of no more than 245 degrees, partial material，such as crystal at high temperature easy to occur the package rupture, cause unable to play the problem, and then affect the function of the product, The temperature can be set using the curve shown in table 6-1.

Table **错误！文档中没有指定样式的文字。**-8 Set temperature curve

Lead-free process temperature curve		
Stage	Temperature	time
Preheat	Temperature rise from room temperature to 150	rate of temperature rising<3℃/s
keep warm	150℃~200℃	40~110 S
Welding	<217℃	40~70 S
	<230℃	15~45 S
	Peak temperature	MAX：245℃
		MIN：230℃





PWI= 74%	Maximum temperature ascending slope		Maximum temperature descending slope		Preheat time 150200C		Time of the reflow temperature or above271C		Upper limit		Total time	/230C
Module edge point	1.3	-34%	-1.9	55%	49.6	-72%	57.4	16%	238.7	16%	29.5	-3%
Module bottom	1.3	-35%	-1.8	60%	49.1	-74%	56.2	8%	238.1	8%	28.2	-12%
Chip	1.4	-29%	-2.1	46%	52.7	-64%	63.6	57%	242.5	66%	39.6	64%
Temperature difference	0.1		0.3		3.6		7.4		4.3		11.4	

Process limit

Butter of antimony: Define Your Own Spec

Statistic name	Lower limit	Upper limit	Unit
Maximum temperature ascending slope (target: 2.0) (Time distance = 20 seconds)	0.0	3.0	Degree per second
Maximum temperature descending slope (Time distance = 20 seconds)	-5.0	-1.0	Degree per second
Preheat time 150200C	40	110	Seconds
Time of the reflow temperature or above271C	40	70	Seconds
Maximum temperature	230	245	Degree centigrade
Time of the temperature above 230C	15	45	Seconds

Figure错误！文档中没有指定样式的文字。**-9**Reference temperature curve